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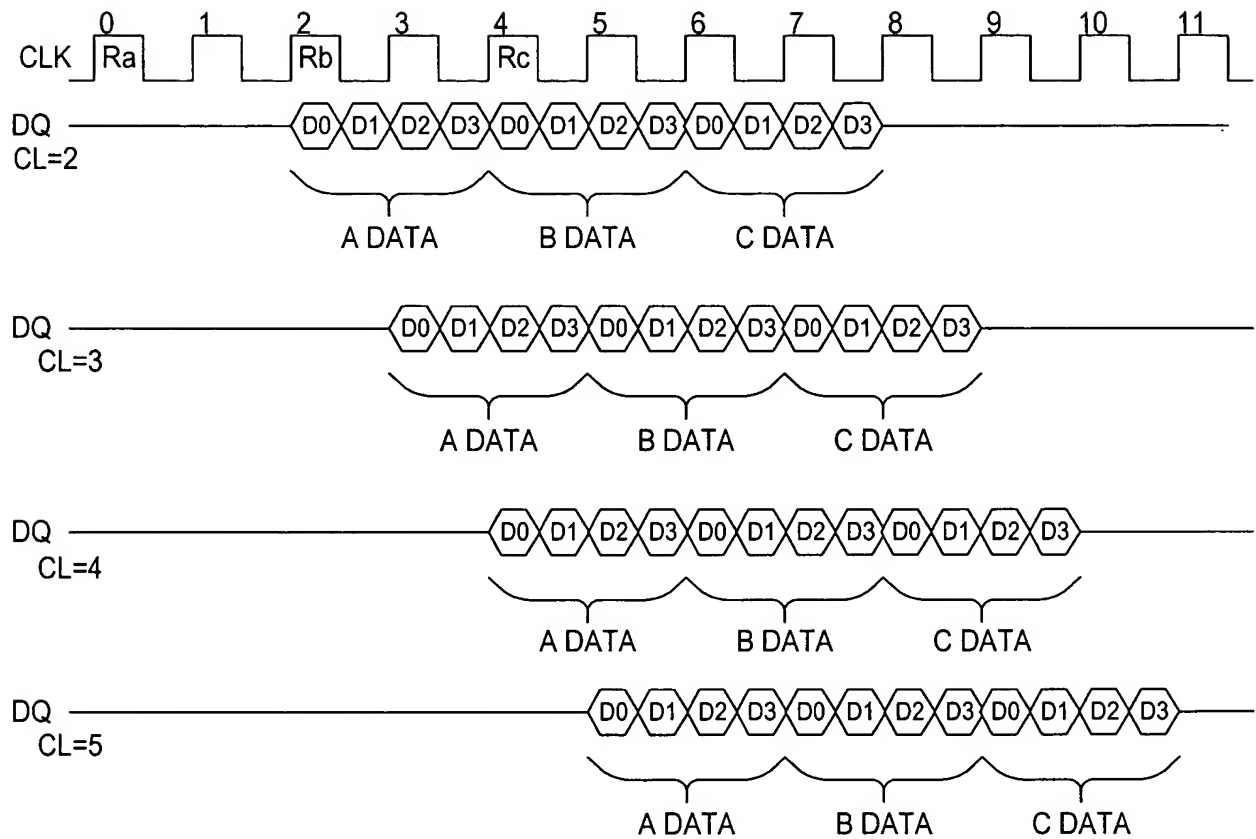


FIG. 1 PRIOR ART

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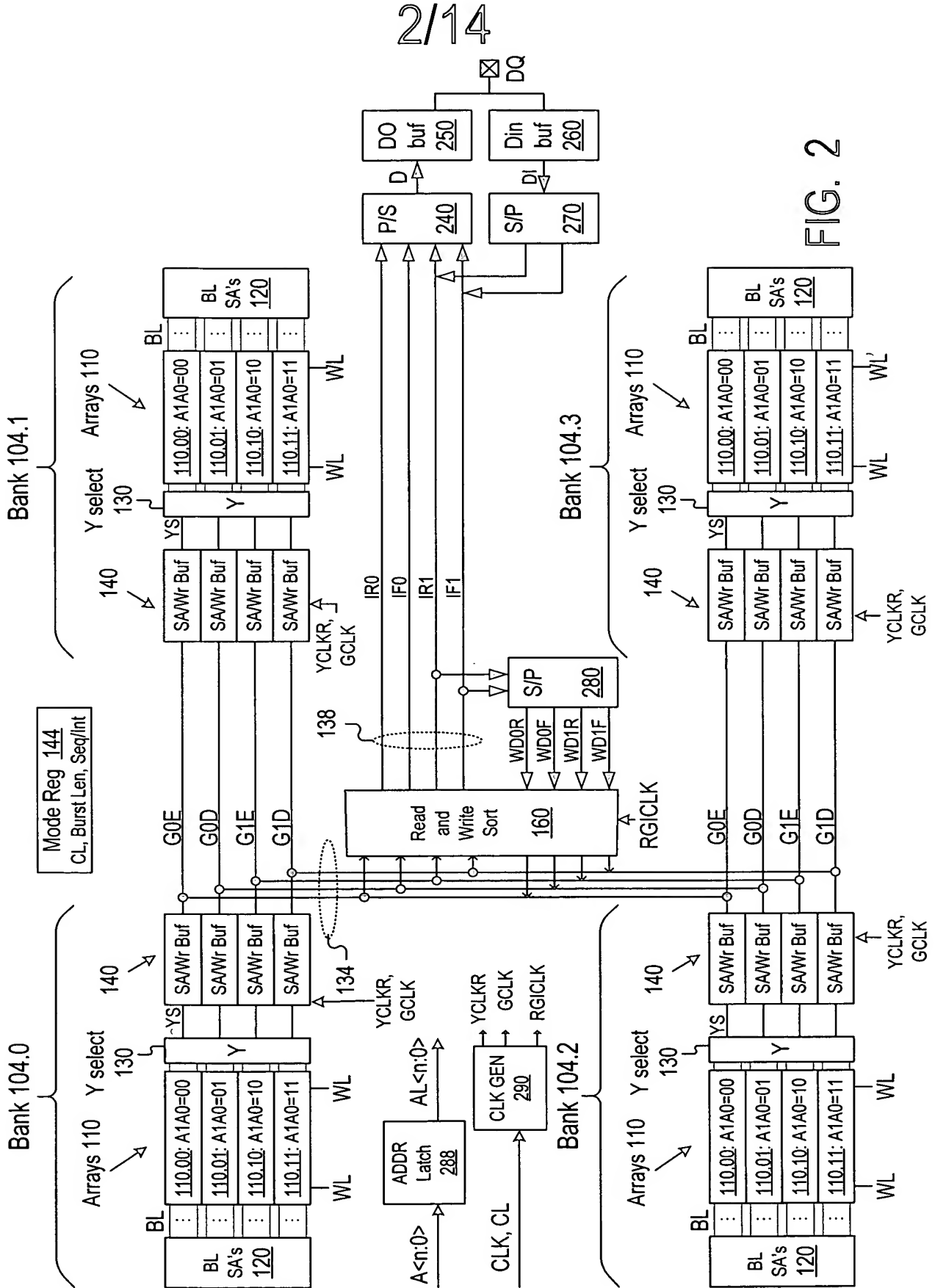
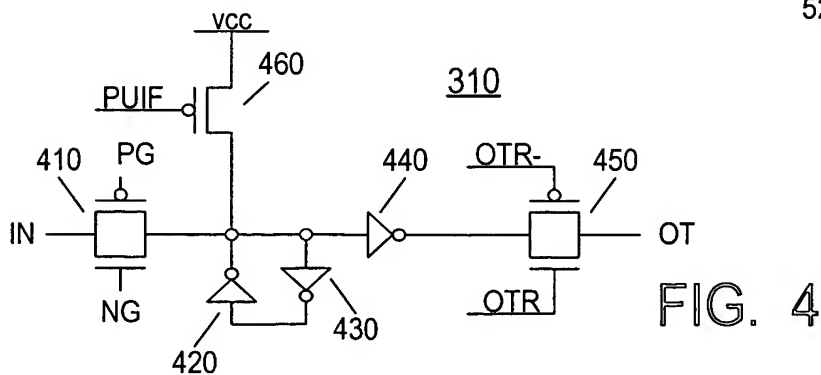
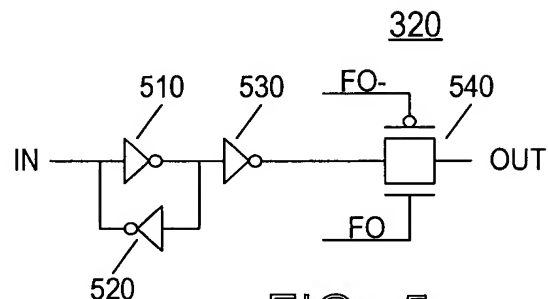
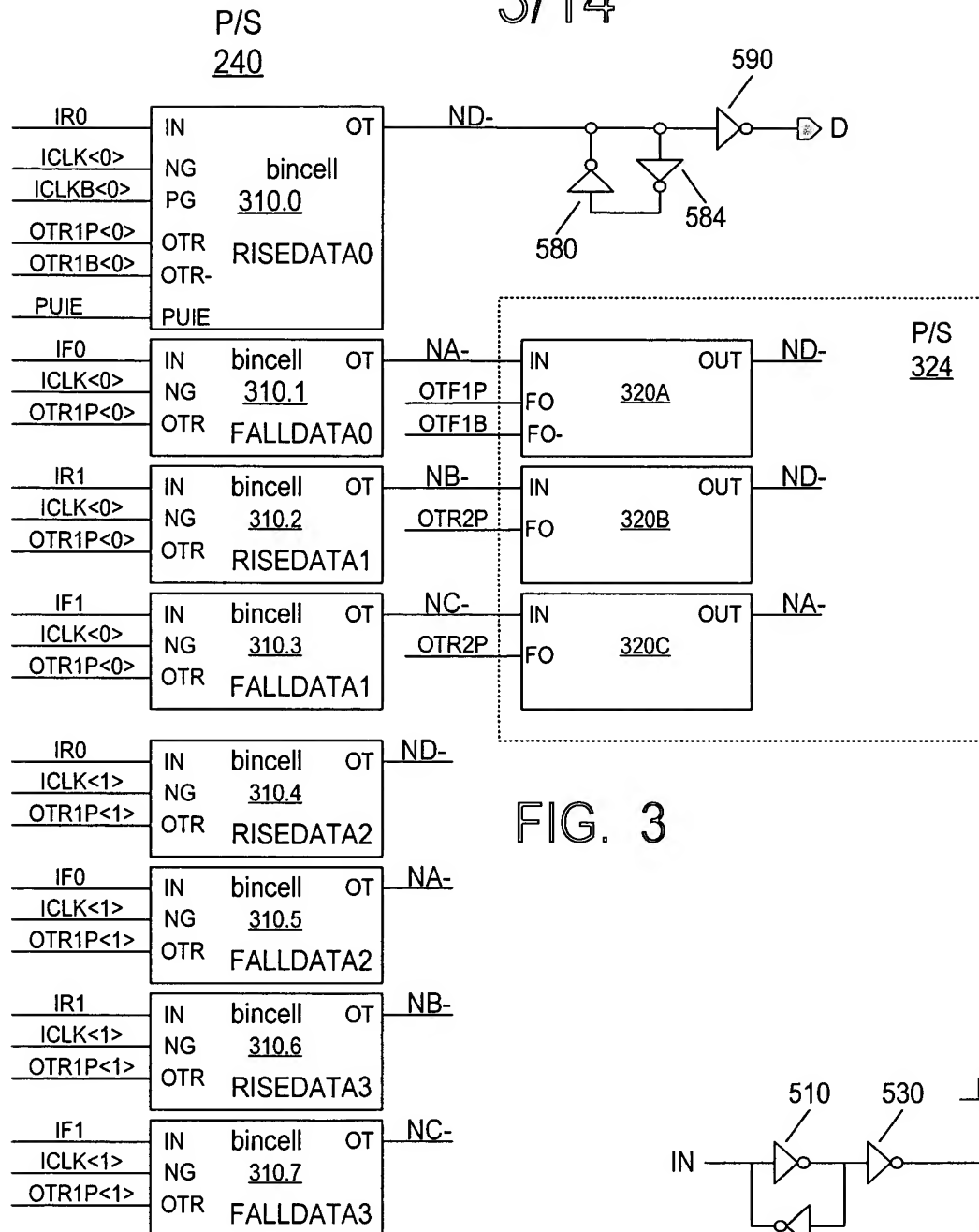


FIG. 2

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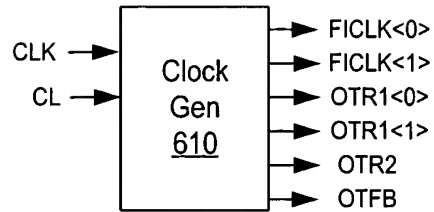


FIG. 6A

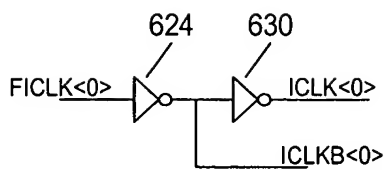


FIG. 6B

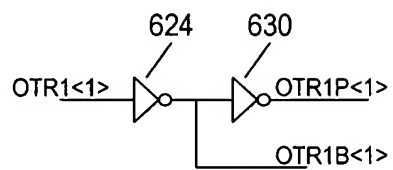


FIG. 6E

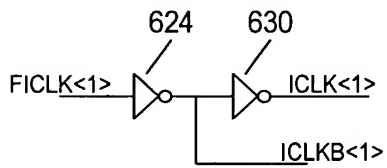


FIG. 6C

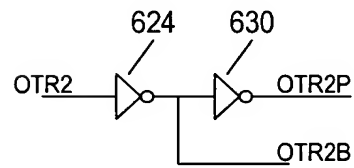


FIG. 6F

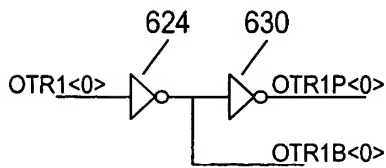


FIG. 6D

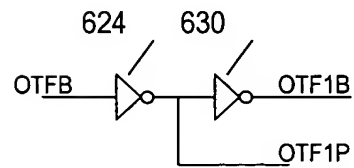


FIG. 6G

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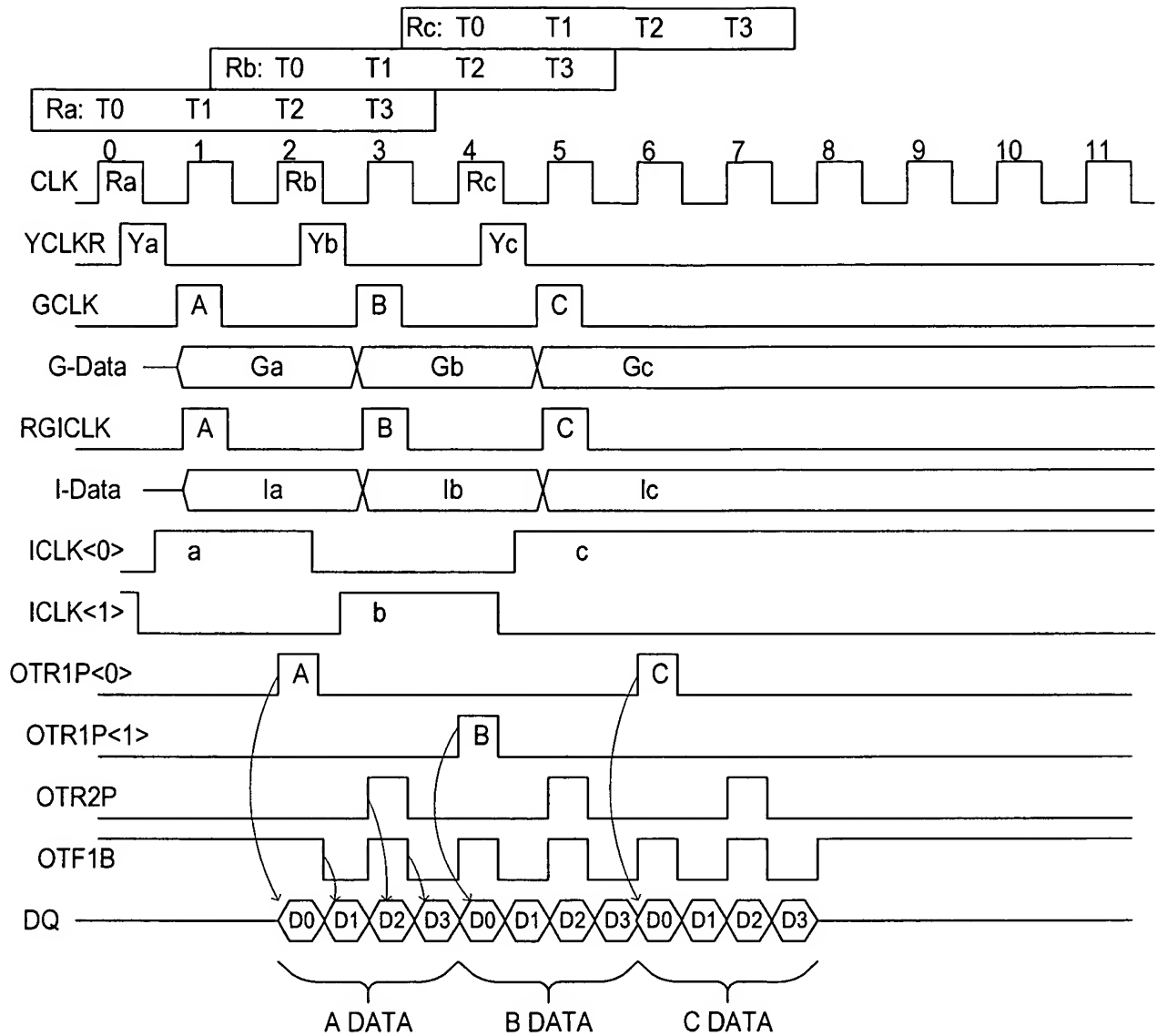
DDR2 CL=2 READ

FIG. 7

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DDR2 CL=3 READ

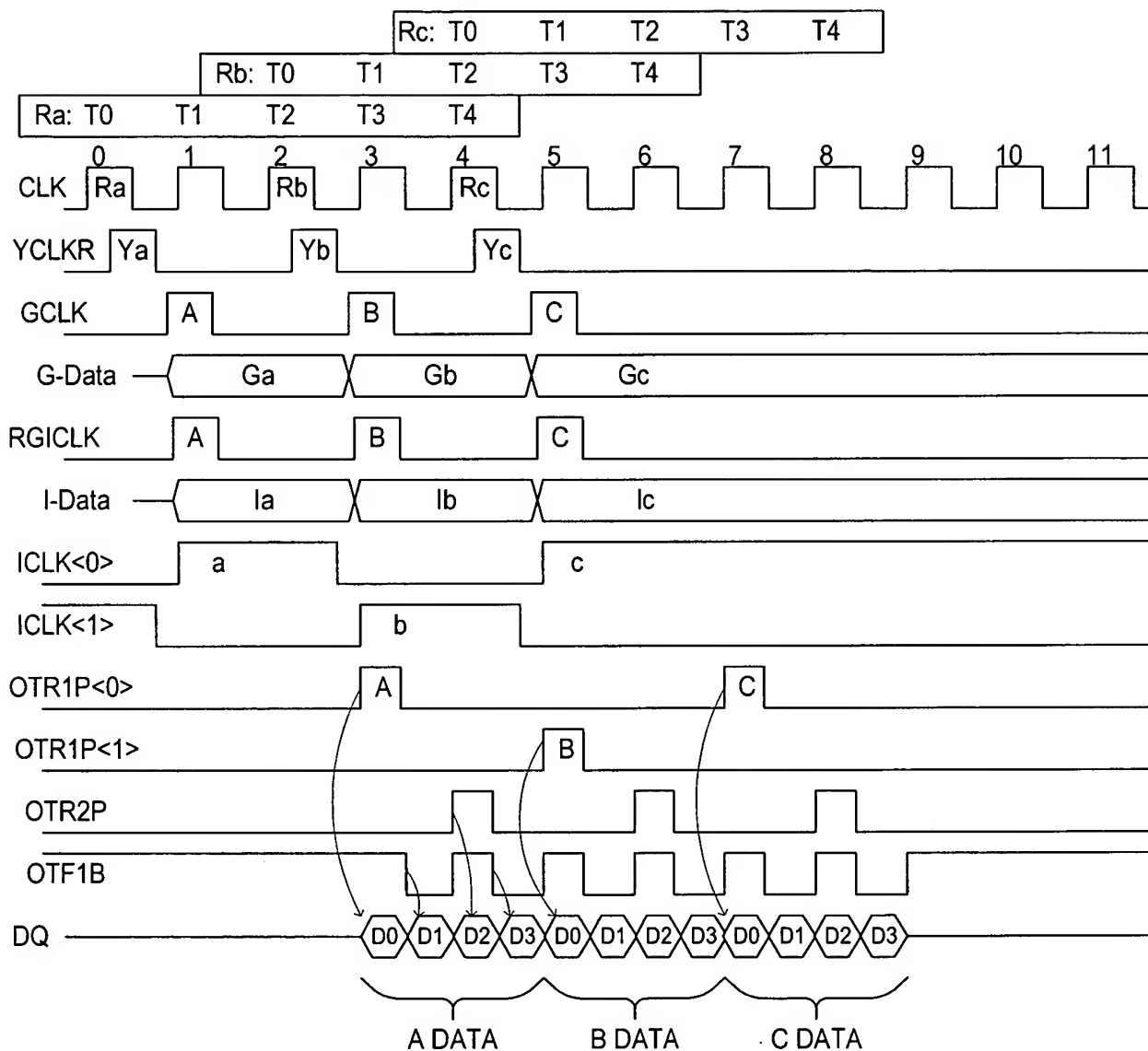


FIG. 8

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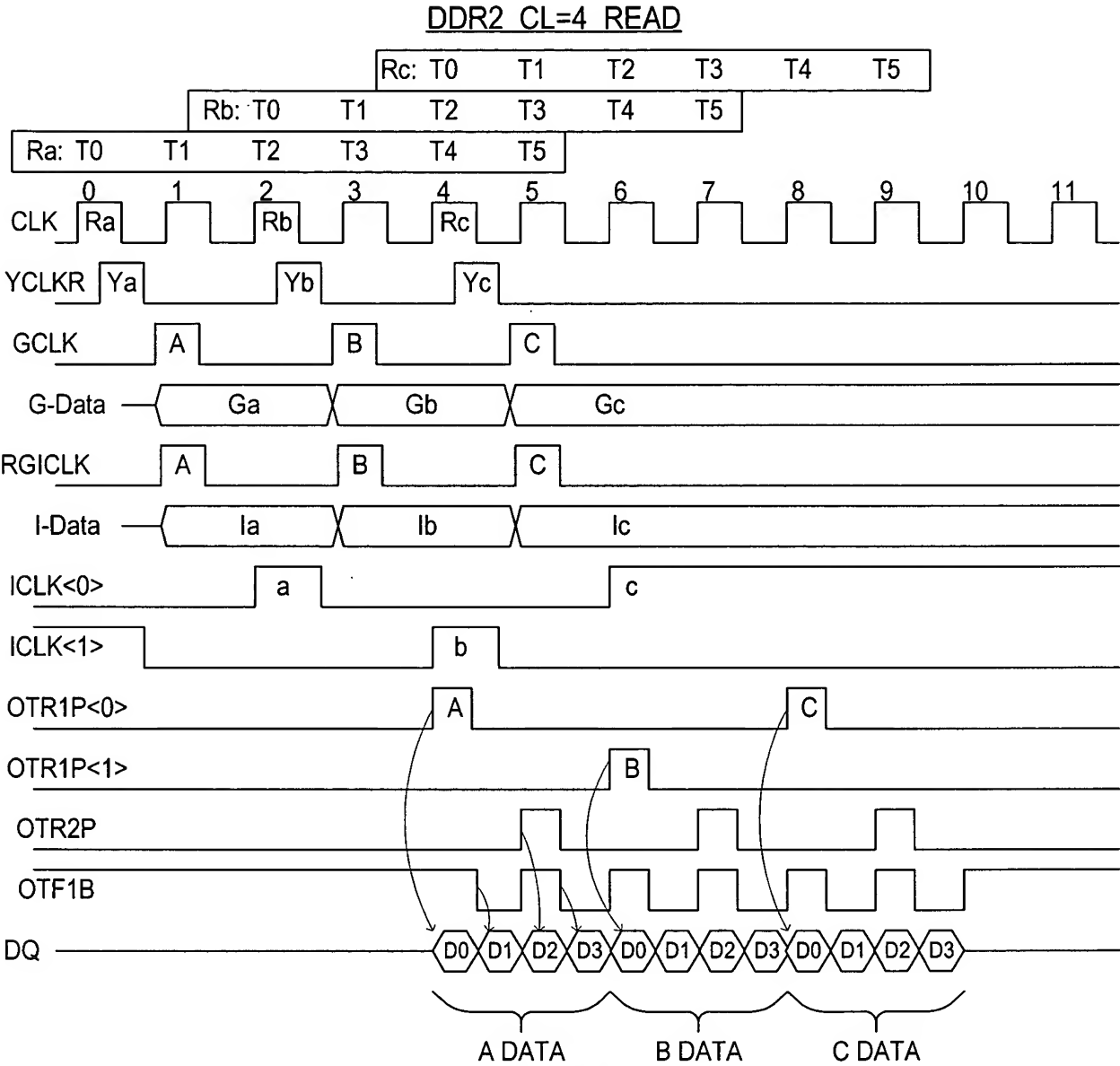


FIG. 9

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DDR2 CL=5 READ

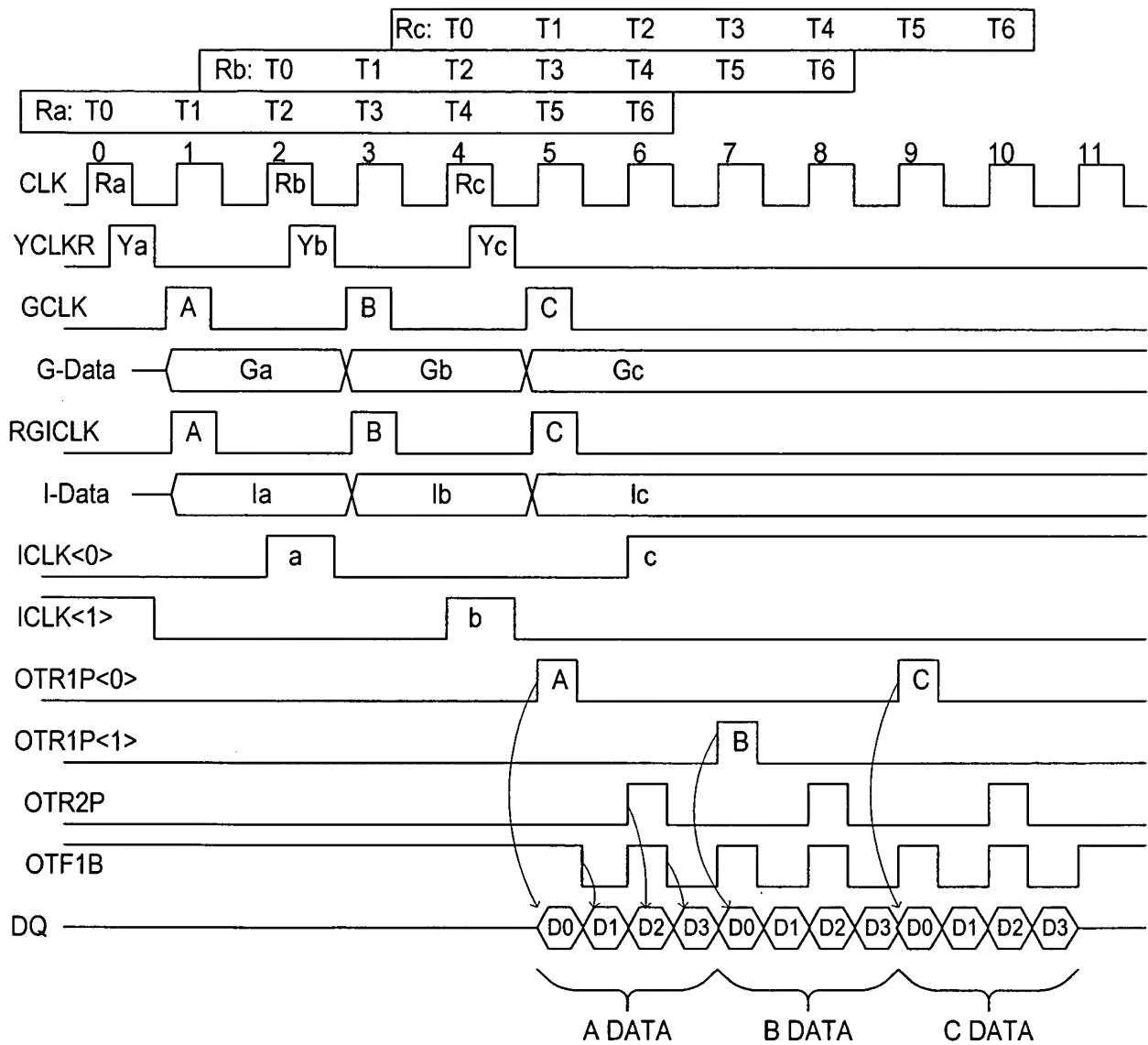


FIG. 10

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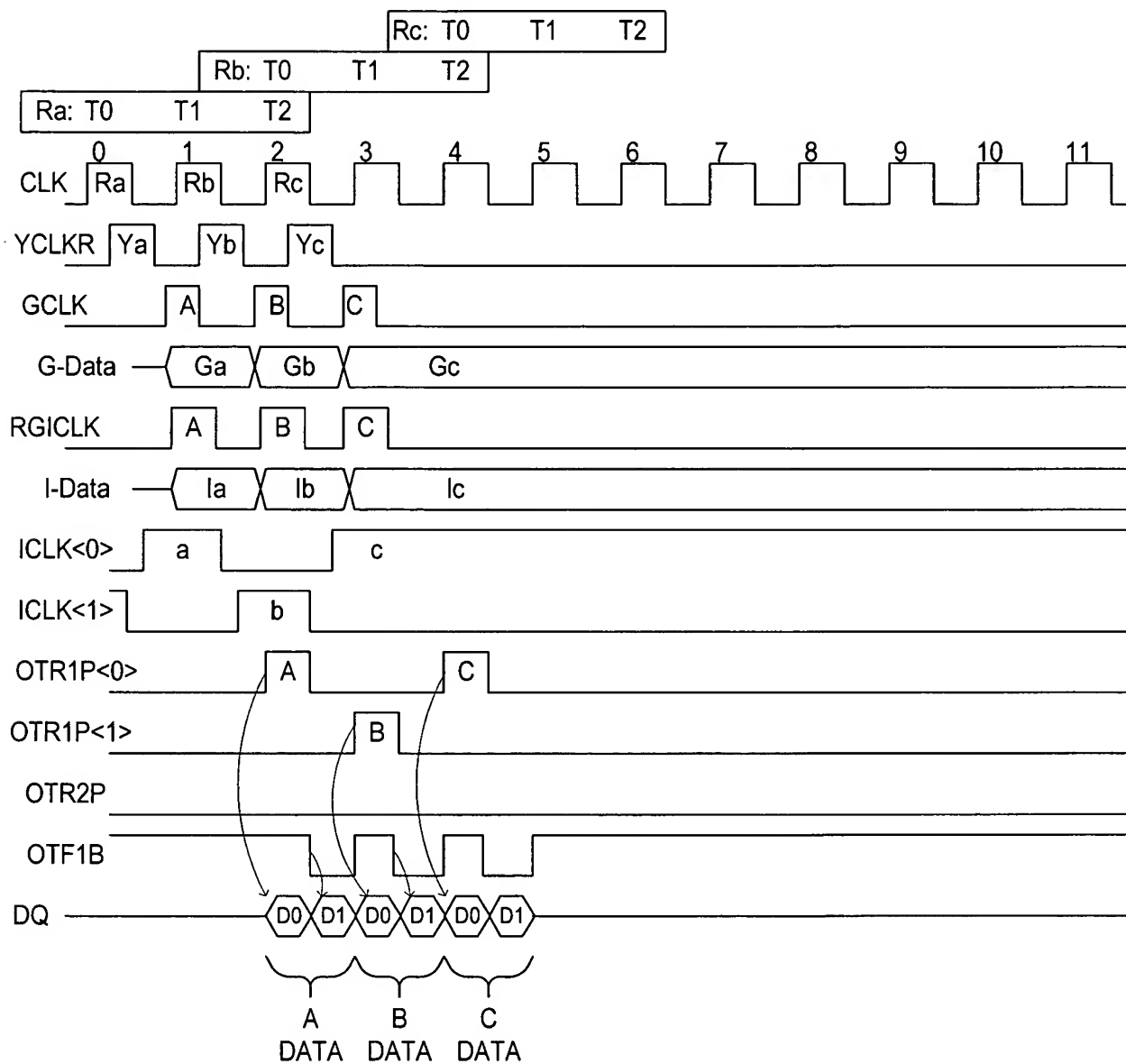
DDR1 CL=2 READ

FIG. 11

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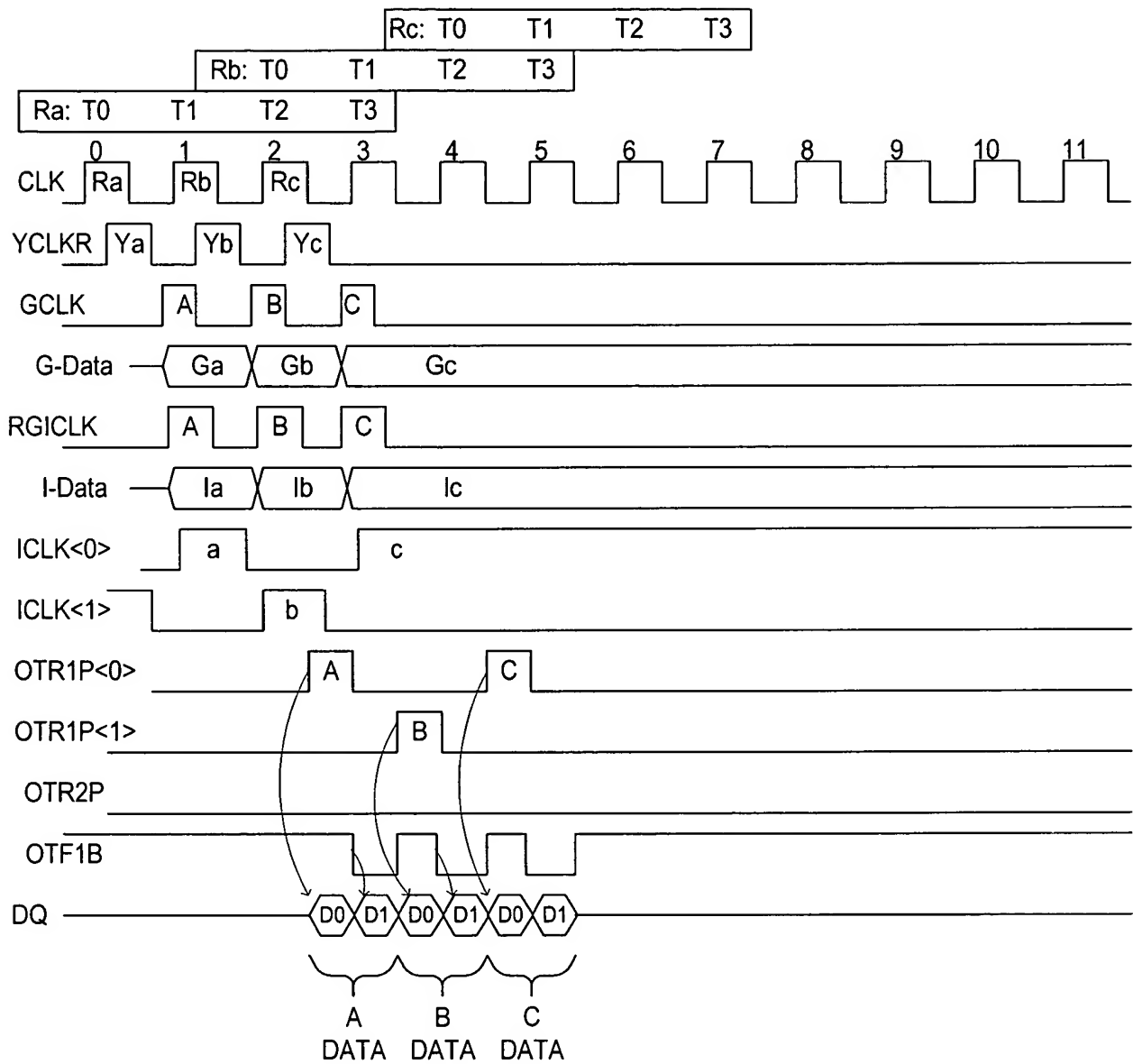
DDR1 CL=2.5 READ

FIG. 12

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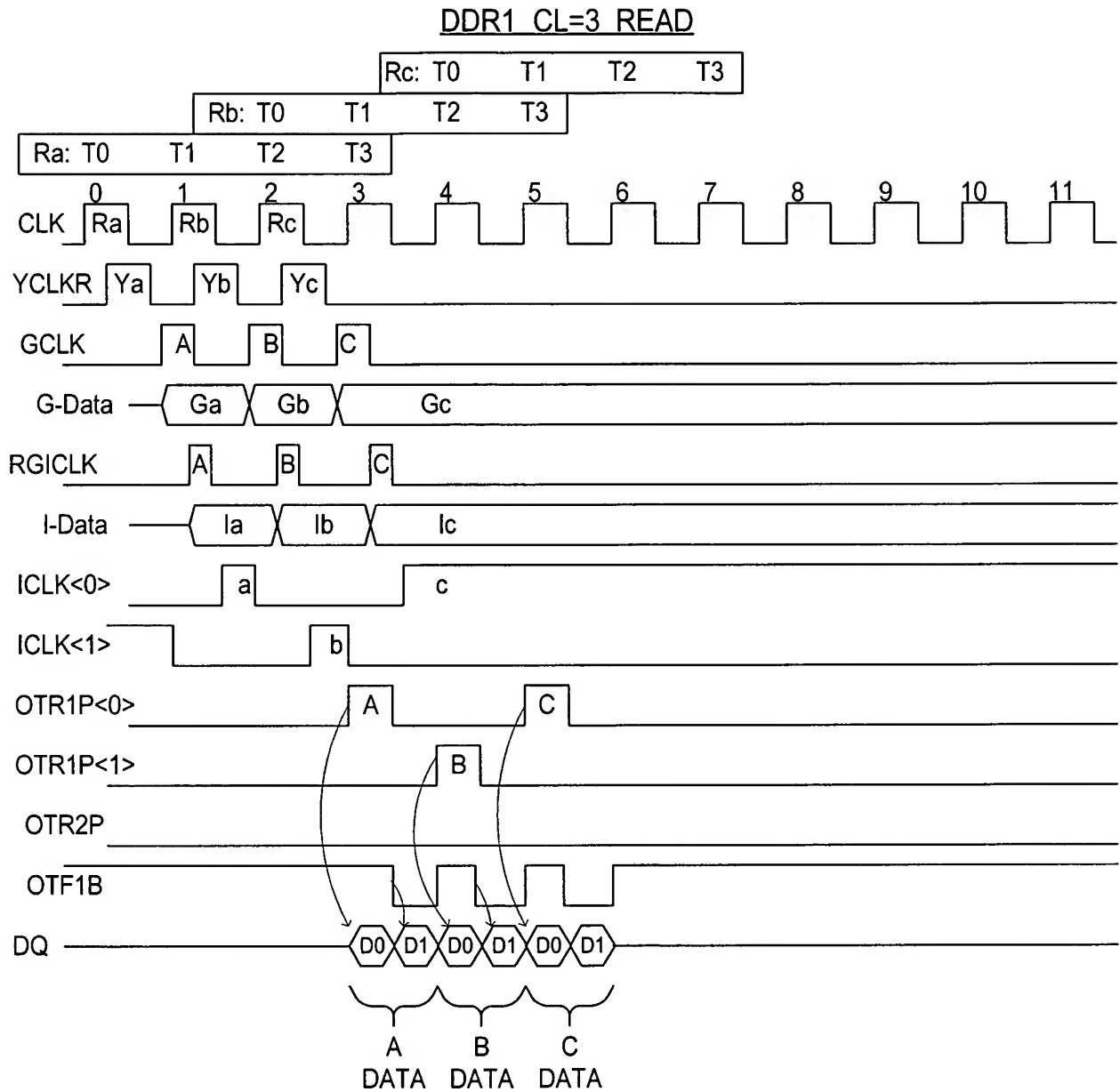


FIG. 13

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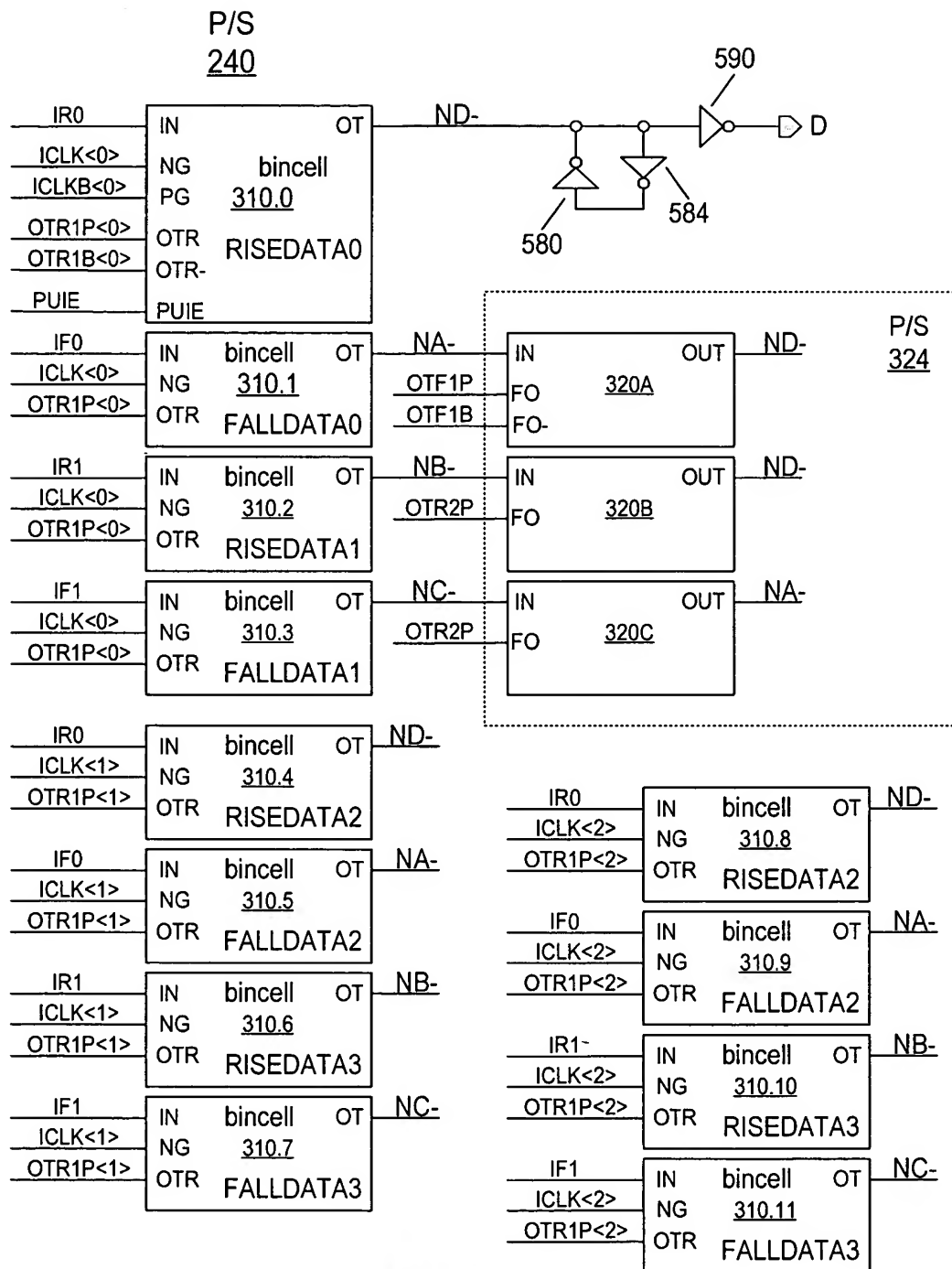
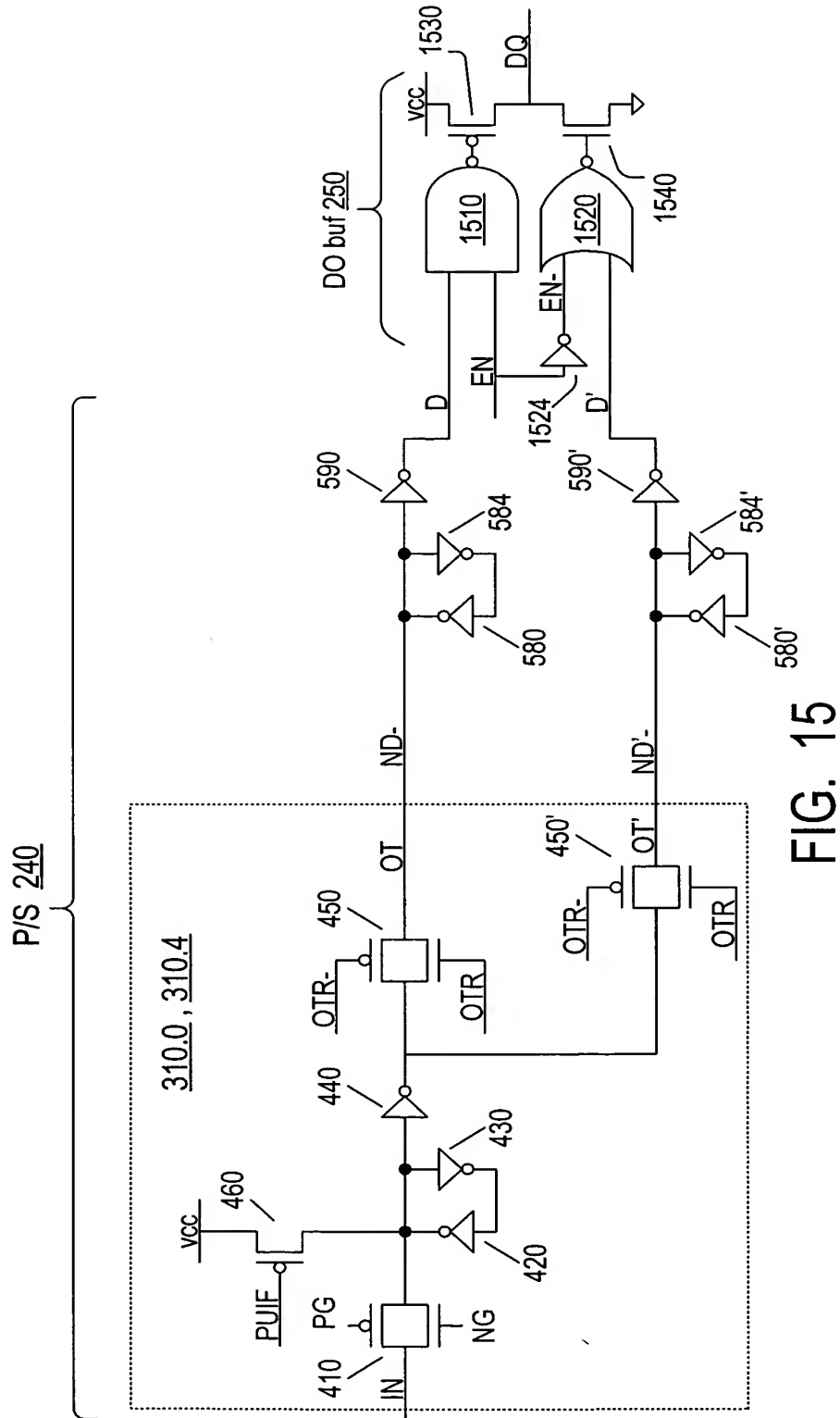


FIG. 14

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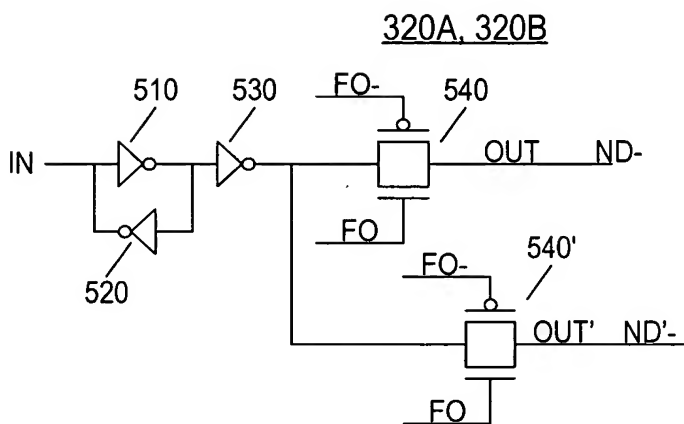


FIG. 16

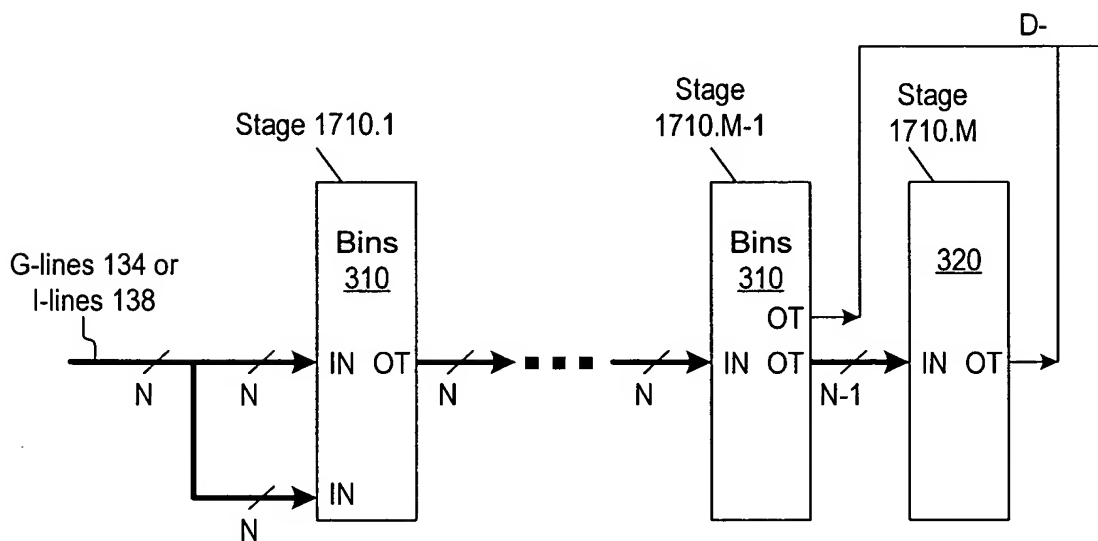


FIG. 17